Design Methodology of High Performance On-Chip Global Interconnect Using Terminated Transmission-Line

Yulei Zhang\textsuperscript{1}, Ling Zhang\textsuperscript{2}, Alina Deutsch\textsuperscript{3}, George A. Katopis\textsuperscript{4}
Daniel M. Dreps\textsuperscript{5}, James F. Buckwalter\textsuperscript{1}, Ernest S. Kuh\textsuperscript{6}, Chung-Kuan Cheng\textsuperscript{2}
\textsuperscript{1}ECE Dept., \textsuperscript{2}CSE Dept., University of California, San Diego, CA
\textsuperscript{3}IBM T. J. Watson Research Center, Yorktown Heights, NY, \textsuperscript{4}IBM System Group, Poughkeepsie, NY
\textsuperscript{5}IBM System and Technology Group, Austin, TX, \textsuperscript{6}University of California, Berkeley, CA
\textsuperscript{1}y1zhang@ucsd.edu, \textsuperscript{2}lizhang@cs.ucsd.edu
\textsuperscript{3}deutsch@us.ibm.com, \textsuperscript{4}katopis@us.ibm.com, \textsuperscript{5}drepsdm@us.ibm.com
\textsuperscript{1}buckwalter@ece.ucsd.edu, \textsuperscript{6}kuh@eecs.berkeley.edu, \textsuperscript{2}ckcheng@ucsd.edu

Abstract — We explore two schemes using transmission-line (T-line) to achieve high-performance global interconnects on VLSI chips. For both schemes, we select wire dimensions to ensure T-line effects present and employ inverter chains as drivers and receivers. In order to achieve high throughput and alleviate Inter-Symbol Interference (ISI), high termination resistance is used in the second scheme. For the two schemes, we discuss how to optimize the wire dimensions and the effects of driver impedance and termination resistance on the wire bandwidth. Secondly, design methodology is proposed to determine the optimal design variables for three objectives. We adopt the proposed methodology and compare the performance metrics with repeated RC wires. Simulation results show that, the proposed T-line schemes reduce the delay and improve the throughput as much as 82\% and 63\%, for min-ddp (delay$^2$-power product) objective.

Keywords — On-chip transmission line, global interconnect, termination resistance, design methodology

I. Introduction

As the semiconductor technology advances, the interconnection becomes a critical factor to determine the digital system performance and the power consumption. According to the prediction of ITRS roadmap 2007 \cite{1}, at 45 nm technology node, the RC delay is 542 ps for 1 \textmu m minimum pitch Cu global wire, whereas the clock frequency will reach 10 GHz (equivalent to 100 ps cycle time). So, there exists a huge performance gap between the interconnect delay and required clock rate. Interconnects, especially the global wires, also consume a significant portion of total power. In \cite{2}, Magen \textit{et al.} found that interconnection power accounts for half the total dynamic power of a 0.13 \textmu m microprocessor, and nearly 50\% of the interconnect-power is consumed by global wires.

To improve the global wire delay, buffer/repeater insertion is normally used nowadays, which is referred as \textit{repeated RC wires} \cite{3}. By repeatedly inserting buffers along the long wire, the wire is divided into several RC segments, which reduces the load driven by each buffer, making the total delay change linearly w.r.t the wire length. How to design such repeated wire structure under different objective functions has been well studied in previous works \cite{4}, \cite{5}, \cite{6}. Although buffers improve the wire performance, they also bring the overhead in terms of extra power consumption, chip area and wiring complexity. In \cite{6}, Zhang \textit{et al.} pointed out that, to minimize the total delay, the gate capacitance of buffer should be equal to the wire segment capacitance, which means that half of the dynamic power is dissipated on buffers.

As a potential alternative, on-chip global wiring using transmission line (T-line) has attracted many research focus recently. It has been shown in \cite{7} that, under some conditions, transmission line effects need to be considered for on-chip wires. If the wires are operated in LC-region, the wire delay will be determined by the wave propagation delay, which is much smaller than the wire RC delay. Wave propagation also reduces the power consumption by eliminating the full-swing charge and discharge on wire and gate capacitance. However, on-chip T-lines normally need larger dimension than RC wires, and could encounter Inter-Symbol Interference (ISI) brought by resistive loss, which makes T-line structures not cost efficient in terms of throughput density. To break this barrier, various approaches have been proposed. \cite{8}, \cite{9} added termination resistance to minimize the distortion and derived the analytical formula for optimal resistance value. \cite{10}, \cite{11} utilized passive and active equalization to alleviate the ISI. \cite{12}, \cite{13}, \cite{14}, \cite{15} adopted different transceiver schemes on long global wires, and the overall performance is compared with repeated RC wires.

In this work, we explore two T-line schemes for achieving high-performance on-chip global interconnects. The first scheme adopts tapered inverter chain (equal size-progressive ratio) as the driver and receiver of long global wire, which is based on the work of \cite{7} and \cite{16}. By choosing larger wire geometry and proper driver impedance, this scheme could achieve better performance compared with repeated RC wires in terms of total delay and Far-End Noise (FEN). However, this scheme cannot achieve high throughput because of the full-swing signal at wire end. In order to push the scheme for higher bandwidth, we add the termination resistance at the far-end of T-line and devise a non-tapered inverter chain (shown later) to amplify the received small signal back to full-swing. The two T-line schemes are designed and simulated, and the performance...
metrics including delay, power, throughput are compared with repeated RC wires under different objectives.

Our contributions of this work include: 1) A new on-chip global interconnect structure using terminated transmission line and non-tapered inverter chain as transceiver, 2) A design methodology to achieve unified design of termination resistance and inverter chain in proposed interconnect structure, 3) A case study using predictive 45 nm process to verify the potential of proposed structure, which is also compared with repeated RC wires under different design objectives.

The rest of this paper is organized as follows. Section II introduces the two schemes we study in this work, and discusses how to choose the wire dimension and driver impedance according to T-line theory. Furthermore, Section III describes the design methodology for these two schemes respectively, emphasizing the determination of the bandwidth of the T-line scheme with termination resistance. We utilize these methodologies to design T-line schemes, and summarize all the results in Section IV. The performance metrics are also evaluated and compared with repeated RC wire in this section. Finally, Section V concludes the whole paper.

II. On-Chip Global Interconnect

The two global signaling schemes using T-lines are shown in Figure 1. For both schemes, we adopt single-ended T-line structure and two identical inverter chains as the driver and receiver. We add the termination resistance on the second scheme to push for higher bandwidth. The two schemes are designed to be repeatable, so the total delay and power consumption are contributed by the T-line and following receiver, as shown in the box surrounded by dash line. The detailed features of the two schemes will be discussed in the following sections.

A. Interconnect schemes using T-lines

The scheme without adding termination resistance is shown in Figure 1(a), which follows the structure in the work [7] and [16]. For identification, we refer this scheme as T-line Scheme A. In Scheme A, tapered inverter chain is adopted such that the size of inverters are progressively increasing, which provides a low impedance \( R_s \) to drive the T-line for high-bandwidth (shown later in Section II-C). Like conventional repeated wire design, it must be guaranteed that full-swing signal is received at the T-line output, which limits the overall bandwidth of Scheme A.

By adding the termination resistance \( R_{\text{Load}} \), we get the other signaling scheme, which is referred as T-line Scheme B. Termination resistance lowers the DC voltage of wire output, to match the attenuated high-frequency component of input signal as discussed in [8], resulting in considerable far-end eye-opening at high data rate. The inverter chain used in Scheme B is not simple tapered chain. It consists of an equal-sized chain and a tapered chain, as shown in Figure 1(b). Here, we use the equal-sized inverter chain at first stage of receiver in order to recover received high-speed low-swing signal back to full-swing, then the following tapered chain will improve the slew rate and provide low impedance to drive the T-line. By simulation, we found that two-stage equal-sized inverters are enough for recovering the signal as long as the far-end eye-opening is larger than the threshold of this equal-sized inverter. In this situation, output slew of the first inverter limits the bandwidth of whole inverter chain. Because the output slew of the first inverter is related to worst-case eye-opening, which is determined by bit rate, optimal cycle time \( T_C \) need to balance the bandwidth of T-line and the inverter chain receiver. This issue will be discussed in the Section III.

B. On-chip T-lines

Given the fact that on-chip T-line is very lossy due to the miniaturization of the wire cross section, it can either operate in RC or LC region under different frequen-
cies [17]. In RC region, the frequency is low which makes \( \omega L \ll R \), so the propagation constant could be written as \( \gamma = \frac{\sqrt{2 \pi RC}}{\lambda} + j \frac{\omega RC}{\lambda} \). In this situation, high frequency components of signal travel fast but with more attenuation, resulting in the distortion of received signal and limiting the bit rate. If the frequency increases such that \( \omega L \gg R \), the wire operates at LC region and the propagation constant becomes \( \gamma = \frac{R}{2\sqrt{L/C}} + j\omega \sqrt{LC} \). Therefore the attenuation constant is

\[
a = \frac{R}{2\sqrt{L/C}} = \frac{R}{2Z_0}
\]

where \( Z_0 \) is the characteristic impedance of T-Line, and the phase velocity \( v = \frac{c}{\gamma} = \frac{1}{\sqrt{LC}} \). In LC region, all frequency components of signal will travel with the same speed and get the same attenuation, which achieves the fast distortionless communication.

In reality, on-chip global wires normally have lengths of 5-10 mm, which satisfies that \( l \approx \lambda \) or \( T_{of} \approx t_r \) (\( T_{of} \) is the time of flight, and \( t_r \) is the input signal rise time) as the operation frequency goes up to tens of gigahertz. The wire resistance is kept low such that \( R < \omega L \), so the inductive effects need to be taken into account. The voltage step response of such wire can be expressed as [7]

\[
V(l, t) = [1 - e^{-\frac{l}{\sqrt{Z_0}}} + B(l, t)] u(t - T_{of})
\]

(2)

where \( B(l, t) \) is a slowly rising modified Bessel function. In order to utilize the fast transition of LC-mode, we need to make the first term in (2) dominant, that means we need to keep the resistance attenuation low and increase the incident wave amplitude, which are summarized into several conditions [16]

\[
\begin{align*}
T_{of} &\geq 0.5t_r \\
R/2Z_0 &< 1 \\
R_S &< Z_0
\end{align*}
\]

(3)  (4)  (5)

In this work, we use the single-ended strip line structure to model on-chip T-lines, which has been shown in Figure 2. The ground planes on top and bottom are used to represent different layers while calculating the wire capacitance and inductance, and we put 3 signal lines within power-ground bars to study the crosstalk effects. Due to the skin effect (The skin depth of copper is 0.65 \( \mu m \) at 10 \( GHz \)) and other non-ideal factors, resistance and inductance of on-chip T-line are frequency dependent, especially in the high-frequency region. Therefore, we need to extract the frequency dependent RLGC parameter of the wire using EM filed solver in order to capture the T-line characteristics. Also, some assumptions are introduced to simplify the extraction as shown below:

1) The random switching activity of signal lines on top and bottom orthogonal layers (layer \( n+1 \) and \( n-1 \) if T-line is located on layer \( n \)) do not change the capacitance of T-line due to the statistical cancellation of opposite switching directions, so the ground plane is used to represent orthogonal layers while extracting the T-line capacitance.

2) The power/ground wires on the layer \( n+2 \) and \( n-2 \), which are parallel with T-line on layer \( n \), should be considered as the current return paths while calculating the inductance, so the ground plane is used to represent these parallel wires while extracting the T-line inductance.

The dimension and other parameters of the T-line are summarized in Table I. The two wire cases shown in the table are typically used for global signaling across several millimeter range. The wire length is chosen to be 5 mm to represent the critical path between CPU and cache.

### C. Effects of driver impedance and termination resistance

For scheme A, since we guarantee the full-swing signal at the wire output, the wire bandwidth is defined as [16]

\[
BW = \frac{1}{2.64 \times t_r}
\]

(6)

where \( t_r \) is the wire output slew. As discussed before, driver impedance determines the amplitude of incident wave, so it affects the wire output slew and bandwidth as a result. The relation between driver impedance \( R_S \) and wire bandwidth is shown in Figure 3. In this figure, the higher bound of \( R_S \) is set to be the characteristic impedance \( Z_0 = 40 \ \Omega \), whereas the lower bound is chosen to be 10 \( \Omega \) for achievable on-chip inverter size. For both wire cases, reducing \( R_S \) will increase the wire bandwidth, especially for the 16X wire because of the low resistive attenuation. While \( R_S = 10 \ \Omega \), the bandwidth of 16X wire can go up to 14 \( GHz \).

For Scheme B, driver impedance not only affects the wire bandwidth but also determines the eye-opening at wire output together with the termination resistance \( R_{Load} \). Figure 4 shows the 2D map of worst-case eye-opening of 16X wire under different data rates within the design space \( \{R_S, R_{Load}\} \). Generally, eye-opening reduces as the frequency goes high due to the distortion and ISI. Lowering \( R_S \) improves the eye by reinforcing the incident wave and sharpening the rise edge of output signal. On the other hand, given bit rate and driver impedance, there exists an optimal \( R_{Load} \) value in terms of largest eye-opening.
Fig. 4. The effects of driver impedance and termination resistance on eye-opening for Scheme B.

While designing such scheme, it always need to guarantee that worst-case eye is larger than the following inverter threshold voltage, which is around 250-300 mV for most processes.

In summary, lower driver impedance and larger wire cross section are needed in order to achieve high-throughput both for Scheme A and B. As a result, we choose $R_S = 10 \, \Omega$ and 16X wire in the following experiments.

III. Design Methodology

The design methodologies of two T-line schemes are introduced in this section, respectively.

A. T-line Scheme A

In this case, since the wire dimension and driver impedance have been chosen, we take two steps to determine the design variables, which include the first inverter size $S_1$ (ratio to the minimum-size inverter) and number of stages $N$.

Step 1: determine the bit rate

By simulation, we found that the inverter chain could support the desired frequency as long as the full-swing signal is guaranteed at the wire end, so the bit rate of Scheme A is limited by the wire bandwidth, which is already defined in (6) using wire output slew. For given driver impedance and wire geometry, the bit rate can be determined as shown in Figure 3.

Step 2: choose the optimal design variables

At the bit rate found in Step 1, we explore the design space to determine the optimal variables by sweeping the first inverter size $S_1$ and number of stages $N$ within a physical range, and generate the cost map for three different design objectives: minimum delay ($\text{min-d}$), minimum delay-power product ($\text{min-dp}$) and minimum delay$^2$-power product ($\text{min-ddp}$). The optimal design variables correspond to the lowest points on the cost map.

B. T-line Scheme B

For Scheme B, one more design variable $R_{\text{Load}}$ is added while determining the first inverter size $S_1$ and number of stages $N$. Still, two similar steps are taken to design this scheme, but the bit rate is not that straightforward to be chosen as the one in Scheme A.

Step 1: determine the bit rate

Figure 5 provides a design flow to choose the optimal bit rate for Scheme B. We begin with a lower initial bit rate, such as a larger cycle time $T_C$. At this bit rate, we optimize the termination resistance $R_{\text{Load}}$ in terms of largest worst-case eye-opening $V_{\text{eye}}$, by sweeping the $R_{\text{Load}}$ and applying the algorithm in [18] to predict the worst-case eye-opening. If $V_{\text{eye}}$ is larger than the first inverter threshold, which is set to be 250mV here, then the inverter chain output slew is checked to see if the overall output signal could be recovered. Otherwise, the bit rate needs to be reduced to enlarge $V_{\text{eye}}$ in order to satisfy the threshold constraint. At the next stage, the output slew of the inverter chain is compared with the rise time of input signal (assumed to be 10% of cycle time in this work). If the inverter chain can recover the signal with better slew than the input signal, the cycle time could be reduced further; otherwise, we need to reduce the bit rate to balance the bandwidth of wire and the inverter chain. Finally, the optimal bit rate and corresponding termination resistance $R_{\text{Load}}$ are found after some iterations.

Step 2: choose the optimal design variables

Using the optimal bit rate and $R_{\text{Load}}$ found by Step 1, we explore the design space $\{S_1, N\}$ similarly to the Step 2 while designing Scheme A. Also, the optimal variables are chosen for the objective min-d/min-dp/min-ddp, respectively.
### IV. Experimental Results

At 45 nm technology node, we design T-line scheme A and B using the methodologies introduced in Section III under three different design objectives: min-d, min-dp and min-ddp. Also, the performance metrics of Scheme A and B are compared with repeated RC wires, which are optimized under the same objectives using the approach of [6].

#### A. Experimental settings

We use the 2D EM field solver CZ2D of EIP tool suite from IBM [19] to build the 2D structure of T-line in Figure 2 and extract the frequency dependent RLGC tabular model for 10X wire case listed in Table I. During the extraction, the assumptions introduced in Section II-B are followed to calculate the wire capacitance and inductance, respectively. The dielectric constant $\epsilon_r$, loss tangent $\tan\theta$ and resistivity $\rho_{Cu}$ follow the values shown in Figure 2. HSPICE is adopted to simulate the step response of on-chip T-line, which is utilized to predict the worst-case eye-opening with a C-code package from the work of [18].

The 45 nm predictive transistor model [20], which is a Synopsys level3 MOSFET model, is utilized to build the inverter chain in the T-line Scheme A and B. The design flows introduced in Section III are implemented in PERL and MATLAB to find the optimal design parameters under given objective. We simulate the whole circuit in HSPICE to evaluate the delay and power consumption.

For the repeated RC wires, the minimum pitch of global RC wire is 135 nm and the corresponding aspect ratio (AR) is 2.4 at 45 nm node according to the ITRS roadmap 2007 [1]. The repeater model is extracted using the same 45 nm predictive transistor model. We adopt optimization method proposed in [6] to find the optimal wire dimension (width and spacing), the length between repeaters and the repeater size for the three objectives, then evaluate the performance metrics of repeated global RC wires. The results are verified with HSPICE simulation using the II model to represent the distributed RC wires.

#### B. Definitions of performance metrics

We compare the delay, power consumption and throughput of proposed T-Line scheme with repeated RC wires. For the delay comparison, we define the normalized delay:

$$ delay_n = \frac{propagation \ delay}{wire \ length} $$

where the propagation delay includes the wire delay and gate delay. The gate delay refers to the repeater delay for RC wires and the transceiver (inverter chain) delay for T-Line scheme.

The normalized energy per bit is used to evaluate the interconnect power consumption, which is defined as follows:

$$ power_n = \frac{energy \ per \ bit}{wire \ length} = \frac{power}{bit \ rate \times wire \ length} $$

The bit rate of RC wire is the inverse of propagation delay since one bit is transmitted only after the previous bit reaches destination (here we assume RC wires are not pipelined). For T-Line scheme, the bit rate is determined by the wire bandwidth in Scheme A or by the eye-opening and inverter chain in Scheme B as discussed in Section III.

The normalized throughput is defined as:

$$ throughput_n = \frac{bit \ rate}{wire \ pitch} $$

which reflects the amount of data can be transmitted for a given cross area in a given time interval.

#### C. Optimal solutions and performance comparison

Utilizing the design methodologies proposed in Section III, we perform the experiments and generate the 2-D cost maps for T-line Scheme A and B under three objectives (min-d/min-dp/min-ddp), which are shown in Figure 6 and Figure 7 respectively. For Scheme A, the sweeping range of design variables $\{S_1, N\}$ are set to be [40,300] and [3,6], whereas for Scheme B, they are set to be [60,300] and [4,6]. The lowest points in cost maps correspond to the optimal design variables.

We summarize the performance metrics of T-line Scheme A and B under different objectives and compare the results with repeated RC wire in the Table II. By adopting the on-chip T-line schemes, the normalized delay could be reduced greatly. Under min-d objective, T-line Scheme A and B can improve the delay by 76.9% and 78.0%, respectively. Also, the energy consumed on unit wire length is reduced due to the wave propagation of on-chip T-line. Under min-ddp objective, T-line Scheme A consumes 89.0% energy of repeated RC wires. We can notice that, T-line Scheme B will consume 36.6%-47.2% extra energy compared with Scheme A because of the static power dissipated on termination resistance. Regarding the throughput, although the T-line schemes utilize larger wire dimensions, still the throughput is improved under objective min-dp/min-ddp because of the higher bandwidth achieved by T-line. Under min-dp objective, T-line Scheme A can increase the throughput of RC wire by 5%, which could be further increased up to 88% by introducing the termination resistance.
To better understand the effects of driver impedance $R_S$ and termination resistance $R_{Load}$ in Scheme B, we show the wire step response in Figure 8. As shown in Figure 8(a), larger $R_S$ leads to slower rise edge and lower saturation voltage, resulting in the poor eye quality at the wire output. Choosing $R_S = 10\Omega$, the effect of $R_{Load}$ is shown in Figure 8(b). Larger $R_{Load}$ causes the sharper rise edge but also introduces larger reflections, which could also deteriorate the eye-opening. Balancing the above two scenarios, an optimal $R_{Load}$ (220 $\Omega$ in this case) is chosen to generate the largest eye-opening as a result.

### D. Tradeoff between performance metrics

For Scheme B, there exists a tradeoff between achievable bandwidth and interconnect performance, while choosing the number of stages $N$. We show this relation in the Figure 9 by plotting the cycle time $T_C$ and optimal delay$^2$-power (ddp) product versus number of stages $N$ on the same figure. In previous design of T-line Scheme B, we study the performance metrics in a design space $\{S_1, N\}$ at an optimal bit rate, which is actually the lower bound that such scheme can achieve within this given space. As shown in the Figure 9, higher bit rate can be achieved by increasing stage number in the inverter chain, because the output slew rate is improved further by more stages. The bit rate improvement meets the limitation when stage number $N$ is larger than 7, that is, the highest achievable bit rate is around $30 \text{ Gbps}$ ($T_C=33 \text{ ps}$) for Scheme B. On the other hand, the optimal ddp product increases from $3.16 \times 10^4 \text{ ps}^2 \cdot \text{mW}$ to $7.35 \times 10^4 \text{ ps}^2 \cdot \text{mW}$ while the stage number $N$ changes from 4 to 8, as indicated on the figure. In summary, increasing stage number can improve the bit rate as much as 20% but will also bring about 2.3 times performance overhead in terms of optimal ddp product. Therefore, generally speaking, choosing less stage number will bring better performance with considerable bandwidth from the perspective of a designer.

### E. Crosstalk effects

By adding different PRBS input patterns on adjacent lines, which are quiet in the previous experiments, we investigate the crosstalk effects of two T-line schemes. We choose the optimal design under the min-ddp objective to represent the typical application that achieves tradeoff between performance and power consumption. The simulation results show that, considering the crosstalk effects, the normalized delay of T-line Scheme A and B will increase by 9.6% and 2%, respectively. Due to the adjacent capacitance, the power consumptions also increase by 37.0% and 25.7% for Scheme A and B. It can be seen that, by adding the termination resistance, crosstalk effects could be alleviated because a DC path is added at the wire output. Figure 10 shows the eye-diagrams at the output of wire and inverter chain for Scheme B. Comparing Figure 10(a) and 10(b), we can see that, even adding crosstalk effects, Scheme B could work at original bit rate with little performance overhead in terms of received signal quality. By adding the crosstalk, the eye-opening at wire output is re-
(a) Eye-diagrams w/o crosstalk effects.
(b) Eye-diagrams w/ crosstalk effects.

Fig. 10. Eye-diagrams of Scheme B using solution of min-ddp.

(a) Effect of driver impedance $R_S$ on step response.
(b) Effect of termination resistance $R_{\text{Load}}$ on step response.

Fig. 8. Wire step response of Scheme B.

min-d, min-dp and min-ddp. Compared with optimized repeater RC wire using the same process, T-line schemes could improve the delay, reduce the power consumption and achieve comparable or even higher throughput by utilizing the wave propagation. Adding the termination resistance will increase the bandwidth further due to the reduction of signal distortion with the sacrifice of power consumption overhead. To balance the tradeoff between bandwidth and interconnect performance of T-line scheme, it is preferred to use the inverter chain with less stages. While taking the crosstalk effects into account, the termination resistance will alleviate the performance degradation by adding a DC path at the wire end. Therefore, proposed scheme with terminated T-line provides designer a potential alternative to achieve high-performance, low-power and also robust on-chip global interconnects.

B. Future works

The future works will include how to build a more practical model of on-chip T-lines considering the real three dimensional BEOL (Back End Of Line) stacking interconnects. This practical model needs to take orthogonal wires on the adjacent layers (layer $n \pm 1$) and parallel wires on the sub-adjacent layers (layer $n \pm 2$) into account while extracting the T-line capacitance and inductance. Also, adjacent in-plane power/ground bars should be considered when calculating frequency-dependent inductance. In summary, a practical, three dimensional, frequency-dependent T-line model is needed in the future.
Another possible direction is considering the crosstalk effects during the optimization of design variables. This will need to extend the worst-case eye prediction algorithm, which is currently based on the victim line step response, to handle crosstalk effects. As soon as we could evaluate the eye-quality with considering the crosstalk, a new optimization methodology can be developed to generate more robust designs.

VI. Acknowledgement

The authors would like to acknowledge the support of NSF CCF-0811794 and California MICRO Program.

References


