Integration of Millimeter-wave Components in SOI CMOS Processes

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Motivation and Applications

- **Military Applications**
  - **Challenge with Satellite Front-end Electronics**
    - Should provide high-power (e.g., >1 W) and weight.
    - Each satellite weighs 10,000 lbs.
  - **Low Noise Amplifier**
  - **Passive I/Q Mixer**

- **Commercial Applications**
  - **Credit Card Validation**
  - **ATM/Pay at the Pump**
  - **In-Store Audio**
  - **Broadband Internet Access**
  - **MILSTAR = Military Strategic and Tactical**

Q-Band Low Noise Amplifier

- **Chip microphotograph**
- **Schematic and EM Illustration**
- The chip area is 0.33 mm x 0.40 mm, excluding pads.
- The measured return loss of the IF and LO port is better than -14 dB and -16 dB at 65 GHz.
- The conversion loss is 3.0 dB and gain and phase imbalance is 1 dB, 2 degrees, respectively.
- The mixer results in a gain compression point (P1dB) of 6.5 dBm at 65 GHz.

Single Pole Double Throw Switch

- **Chip microphotograph**
- **Schematic and EM Illustration**
- The gain is 16.1 dB at 46 GHz, 3-dB bandwidth is 10 GHz (5 to 15 GHz), input & output return losses are >10 dB.
- Between 46-50 GHz, the gain is greater than 10 dB and input return loss is greater than 5 dB.
- The IP3 is -3 dBm and OP2 = 14 dBm.
- The gain compression point (P1dB) is 15 dBm, Pout = 2 W, Pout = 2 W.

Comparison Tables

<table>
<thead>
<tr>
<th>Technology</th>
<th>Frequency (GHz)</th>
<th>Gain (dB)</th>
<th>Noise Figure (dB)</th>
<th>P1dB (dBm)</th>
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<tbody>
<tr>
<td>45-nm SOI</td>
<td>43-53</td>
<td>18.5</td>
<td>2.9</td>
<td>22.8</td>
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<tr>
<td>90nm SOI</td>
<td>35</td>
<td>11.9</td>
<td>3.6</td>
<td>40</td>
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<tr>
<td>InP HEMTs</td>
<td>43-45</td>
<td>22</td>
<td>2.1</td>
<td>111</td>
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<tr>
<td>InGaAs HEMT</td>
<td>36-46</td>
<td>20</td>
<td>3.5</td>
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<td>42-47</td>
<td>19</td>
<td>3.1</td>
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</tbody>
</table>

Summary

- **LNA Design for Simultaneous Noise and Power Matching (CICC 2011)**
  - Gain: 2.9 dB NF (state of art), 18.5 dB gain
  - Output P1dB = 2.5 dBm, and OIP3 = 14 dBm.
  - Proper setting of series FET gate width, M1, and shunt FET gate width, M2.
  - Impact of parasitic capacitance: Cgs in the drain region (resistance loss) and Gm2 in the cut-off region (resistance loss).
  - An insertion loss of 1.7 dB, isolation of 25 dB at 45 GHz.
  - The isolation loss and isolation changes 0.3 dB and 0.2 dB when gate control voltage is varied from 0.9 V to 1.1 V.
  - Switching time = 2.1 ns.
  - The insertion loss and isolation changes 0.2 dB and 2 degrees when gate control voltage is varied from 0.9 V to 1.1 V.
  - The gain and phase imbalance is 1 dB and 2 degrees, respectively.

- **SPDT Design for Low Insertion Loss and High Isolation (CSICS 2011)**
  - 50 ohm, 2.5 dB NF (state of art), 15 dB gain, output P1dB = 2.5 dBm, and OP1dB = 14 dBm.
  - 0.5 W power consumption.

- **Phase Shifter Design**
  - 0.5 W power consumption.

- **SOI is a good technology candidate in minimizing the cost and size of the satellite front-end electronics, and will be highly beneficial in highly scaled beamforming and phased array systems.**